

METHOD FOR DYNAMICALLY MODIFYING FREQUENCY IN AN ARITHMETIC UNIT BASED ON ONLINE ERROR DETECTION

Patent Number(s): RO130282-A2 ; RO130282-B1

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Derwent Primary Accession Number: 2015-38362K

Abstract: NOVELTY - The invention relates to a method for dynamically modifying the frequency during the operation of an arithmetic unit within a digital signal processing unit which has adders or multipliers comprised in the critical path. According to the invention, the method consists in dynamically modifying the frequency by the dynamic modification of the clock signal period in an arithmetic circuit (1), based on the detection of the errors due to the delays occurred in the circuit, by a detection contention circuit, using a base 7 residual code.

International Patent Classification: [G06F-001/08](#); [G06F-011/08](#)

Derwent Class Code(s): [T01](#) (Digital Computers)

Derwent Manual Code(s): [T01-G01A](#); [T01-K01](#)

Patent Details:

Patent Number	Publ. Date	Main IPC	Week	Page Count	Language
RO130282-A2	29 May 2015	G06F-001/08	201547		Romanian
RO130282-B1	30 Mar 2018	G06F-001/08	201822		English

Application Details:

RO130282-A2	RO000653	12 Jul 2011
RO130282-B1	RO000653	12 Jul 2011

Priority Application Information and Date:

RO000653	12 Jul 2011
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